

CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

- 1        1. An output stage for a line driver, comprising:
  - 2              a first amplifier comprising a series combination of a first semiconductor device
  - 3              and a second semiconductor device;
  - 4              a second amplifier comprising a series combination of a third semiconductor
  - 5              device and a fourth semiconductor device;
  - 6              a first integrated back-matching resistor network interposed between the first and
  - 7              the second semiconductor devices; and
  - 8              a second integrated back-matching resistor network interposed between the third
  - 9              and the fourth semiconductor devices.
- 1        2. The line driver of claim 1, wherein the first integrated back-matching  
2              resistor network comprises a series combination of integrated resistors having an additive  
3              resistance selected to match an expected load input impedance.
- 1        3. The line driver of claim 2, wherein the second integrated back-matching  
2              resistor network comprises a series combination of integrated resistors having an additive  
3              resistance selected to emulate an expected line input impedance.
- 1        4. The line driver of claim 3, wherein the series combination of integrated  
2              resistors selected to match the expected load input impedance are configured in parallel  
3              with the series combination of integrated resistors selected to emulate the expected line  
4              input impedance.

1       5.     The line driver of claim 4, wherein a supply voltage applied to a source  
2 node of the first and second semiconductor devices of the first and second amplifiers  
3 respectively, is increased to a voltage level exceeding the maximum drain-source voltage  
4 for the semiconductor device technology associated with the first and second  
5 semiconductor devices, resulting in an available maximum power increase at the line  
6 driver output.

1       6.     The line driver of claim 5, wherein the available maximum power increase  
2 at the line driver output is realizable without increasing the maximum current in the line  
3 driver output stage.

1       7.     The line driver of claim 5, wherein the first, second, third, and fourth  
2 semiconductor devices are standard CMOS devices.

1       8.     The line driver of claim 7, wherein the first and third semiconductor  
2 devices are PMOS transistors.

1       9.     The line driver of claim 7, wherein the second and fourth semiconductor  
2 devices are NMOS transistors.

1       10.    The line driver of claim 7, wherein the standard CMOS devices have a  
2 maximum drain-source voltage of approximately 5 Volts.

1       11.    The line driver of claim 10, wherein the power supply maximum voltage is  
2 approximately 20/3 Volts.      9

1       12.    The line driver of claim 11, wherein the effective signal swing across a  
2 load is approximately 10/3 Volts.

1        13. The line driver of claim 11, wherein the effective power gain available at  
2 the output of the line driver is greater than approximately 2.5 dB larger than the effective  
3 power gain of a conventional line driver.

1        14. The line driver of claim 13, wherein the effective power gain available at  
2 the output of the line driver is approximately 3.0 dB larger than the effective power gain  
3 of a conventional line driver.

1        15. An output stage for a line driver, comprising:  
2            a first amplifier comprising a series combination of a first semiconductor device  
3 and a second semiconductor device;  
4            a second amplifier comprising a series combination of a third semiconductor  
5 device and a fourth semiconductor device;  
6            a first integrated back-matching resistor interposed between the first and the  
7 second semiconductor devices and a first line driver output node;  
8            a second integrated back-matching resistor interposed between the third and the  
9 fourth semiconductor devices and a second line driver output node;  
10          a first supply voltage protective semiconductor device interposed in series  
11 between the first semiconductor device and the first integrated back-matching resistor;  
12          a second supply voltage protective semiconductor device interposed in series  
13 between the first integrated back-matching resistor and the second semiconductor device;  
14          a third supply voltage protective semiconductor device interposed in series  
15 between the third semiconductor device and the second integrated back-matching resistor;  
16          and  
17          a fourth supply voltage protective semiconductor device interposed in series  
18 between the second integrated back-matching resistor and the fourth semiconductor  
19 device.

1        16.    The line driver of claim 15, wherein the sum of the resistance values of the  
2    first and the second integrated back-matching resistors is selected to match an expected  
3    load input impedance.

1        17.    The line driver of claim 15, wherein the first and second supply voltage  
2    protective semiconductor devices comprise at least one source follower.

1        18.    The line driver of claim 15, wherein the first and second supply voltage  
2    protective semiconductor devices protect only a respective semiconductor device that is  
3    idle.

1        19.    The line driver of claim 16, wherein the first and second integrated back-  
2    matching resistors have a resistance of approximately the same value.

1        20.    The line driver of claim 19, wherein a supply voltage is increased to a  
2    voltage level exceeding the maximum drain-source voltage for the semiconductor device  
3    technology associated with the first, second, third, and fourth semiconductor devices,  
4    resulting in an available maximum power increase at the line driver output.

1        21.    The line driver of claim 20, wherein the available maximum power  
2    increase at the line driver output is realizable without increasing the maximum current in  
3    the line driver output stage.

1        22.    The line driver of claim 21, wherein the power supply maximum voltage is  
2    approximately twice the maximum drain-source voltage of the semiconductor device  
3    technology of the first, second, third, and fourth semiconductor devices.

1        23.    The line driver of claim 15, wherein the first, second, third, and fourth  
2    semiconductor devices are standard CMOS devices.

1        24. The line driver of claim 23, wherein the standard CMOS devices have a  
2 maximum drain-source voltage of approximately 5 Volts.

1        25. The line driver of claim 24, wherein the power supply maximum voltage is  
2 approximately 10 Volts.

1        26. The line driver of claim 25, wherein the first and third semiconductor  
2 devices are PMOS transistors.

1        27. The line driver of claim 25, wherein the second and fourth semiconductor  
2 devices are NMOS transistors.

1        28. The line driver of claim 25, wherein the first and third supply voltage  
2 protective semiconductor devices are PMOS transistors.

1        29. The line driver of claim 25, wherein the second and fourth supply voltage  
2 protective semiconductor devices are NMOS transistors.

1        30. The line driver of claim 25, wherein the effective signal swing across a  
2 load is approximately equivalent to the full power supply voltage range.

1        31. The line driver of claim 25, wherein the effective power gain available at  
2 the output of the line driver is approximately 6.0 dB larger than the effective power gain  
3 of a conventional line driver.

1       32. An output stage for a line driver, comprising:

2            a first amplifier comprising a series combination of a first semiconductor device, a

3       first semiconductor protective device, a second semiconductor device, and a second

4       semiconductor protective device, wherein the first and second semiconductor protective

5       devices are interposed between the first semiconductor device and the second

6       semiconductor devices;

7            a second amplifier comprising a series combination of a third semiconductor

8       device, a third semiconductor protective device, a fourth semiconductor device, and a

9       fourth semiconductor protective device, wherein the third and fourth semiconductor

10      protective devices are interposed between the third semiconductor device and the fourth

11      semiconductor devices;

12            a first integrated back-matching resistor network interposed between the first

13       semiconductor protective device and a first pole of a transformer;

14            a second integrated back-matching resistor network interposed between the first

15       pole of the transformer and the second semiconductor protective device;

16            a third integrated back-matching resistor network interposed between the third

17       semiconductor protective device and a second pole of the transformer; and

18            a fourth integrated back-matching resistor network interposed between the second

19       pole of the transformer and the fourth semiconductor protective device.

1       33. The line driver of claim 32, wherein the first, second, third, and fourth

2       integrated back-matching resistor networks comprise a combination of integrated resistors

3       having a resistance selected to match an expected load input impedance.

1       34. The line driver of claim 32, further comprising:  
2            a first integrated resistor having a resistance selected to emulate an expected line  
3            input impedance interposed between the first and the second integrated back-matching  
4            resistor networks; and  
5            a second integrated resistor having a resistance selected to emulate an expected  
6            line input impedance interposed between the third and the fourth integrated back-  
7            matching resistor networks.

1       35. The line driver of claim 32, wherein a supply voltage applied to a source  
2           node of the first and third semiconductor devices is increased to a voltage level exceeding  
3           the maximum drain-source voltage for the semiconductor device technology associated  
4           with the first, second, third, and fourth semiconductor devices, resulting in an available  
5           maximum power increase at the line driver output.

1       36. The line driver of claim 35, wherein the available maximum power  
2           increase at the line driver output is realizable without increasing the maximum current in  
3           the line driver output stage.

1       37. The line driver of claim 36, wherein the first, second, third, and fourth  
2           semiconductor devices are standard CMOS devices.

1       38. The line driver of claim 37, wherein the standard CMOS devices have a  
2           maximum drain-source voltage of approximately 5 Volts.

1       39. The line driver of claim 37, wherein the power supply maximum voltage is  
2           approximately 40/3 Volts.

1       40. The line driver of claim 37, wherein the first and third semiconductor  
2           devices are PMOS transistors.

1       41.   The line driver of claim 37, wherein the second and fourth semiconductor  
2 devices are NMOS transistors.

1       42.   The line driver of claim 37, wherein the first and third supply voltage  
2 protective semiconductor devices are PMOS transistors.

1       43.   The line driver of claim 37, wherein the second and fourth supply voltage  
2 protective semiconductor devices are NMOS transistors.

1       44.   The line driver of claim 39, wherein the effective signal swing across a  
2 load is approximately 20/3 Volts.

1       45.   The line driver of claim 39, wherein the effective power gain available at  
2 the output of the line driver is greater than approximately 8.5 dB larger than the effective  
3 power gain of a conventional line driver.

1       46.   The line driver of claim 39, wherein the effective power gain available at  
2 the output of the line driver is approximately 9.0 dB larger than the effective power gain  
3 of a conventional line driver.

1       47.   An integrated circuit line driver, comprising:  
2           means for increasing the effective output signal swing to at least a voltage level  
3           that exceeds the maximum drain-source voltage of the integrated circuit technology.

1       48.   The line driver of claim 47, wherein the means for increasing the effective  
2 output signal swing is accomplished with an integrated resistor network.

1       49.   The line driver of claim 47, wherein the means for increasing the effective  
2 output signal swing is accomplished with a combination of protective semiconductor  
3 devices and a plurality of integrated back-matching resistors.

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1        50.    The line driver of claim 47, wherein the protective semiconductor devices  
2 comprise at least one source follower.

1        51.    The line driver of claim 49 wherein the protective semiconductor devices  
2 protect a semiconductor device that is idle.

1        52.    A transmission unit, comprising:  
2              a line driver having an output stage, wherein the output stage is configured to  
3              transmit a signal having a peak-to-peak voltage swing that exceeds the maximum drain-  
4              source voltage of the integrated circuit technology used to implement the line driver.

1        53.    A communications system, comprising:  
2              a transmission unit having an integrated line driver, the integrated line driver  
3              having an output stage, wherein the output stage is configured to transmit a signal having  
4              a peak-to-peak voltage swing that exceeds the maximum drain-source voltage of the  
5              integrated circuit technology used to implement the line driver.

1        54.    A method of increasing the available signal transmit power on a  
2 transmission line, comprising:  
3              applying a transmit signal to an input stage of an integrated line driver;  
4              amplifying the transmit signal such that the output signal swing exceeds the  
5              maximum drain-source voltage of the integrated circuit technology used to implement an  
6              at least one amplifier in an integrated line driver output stage; and  
7              applying the amplified transmit signal via an integrated resistor network to the  
8 transmission line.

1        55.    The method of claim 54, wherein the integrated resistor network  
2 comprises:  
3              a parallel combination of a first resistor branch comprising an at least balanced  
4              pair of integrated resistors selected to match an expected load impedance.

1        56. The method of claim 54, wherein the integrated resistor network  
2 comprises:

3              a pair of integrated back-matching resistors selected such that the sum of their  
4 resistance values approximates an expected load impedance, wherein each of the  
5 integrated back-matching resistors supplies half of the available signal transmit power to  
6 a load.

1        57. The method of claim 54, wherein the step of amplifying the transmit signal  
2 is accomplished by adding a plurality of protective semiconductor devices, wherein each  
3 of the plurality of protective semiconductor devices protects a corresponding  
4 semiconductor device when the corresponding semiconductor device is idle.

1        58. The method of claim 57, wherein each of the plurality of protective  
2 semiconductor devices comprise at least one source follower.